REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

Claims 1-4 and 7-11 stand rejected under 35 U.S.C. §112 paragraph as being indefinite. Based on the Examiner's suggestions, claims 1, 4, 8, 9, and 11 have been amended. In addition, claim 7 has been canceled. Withdrawal of the rejection under 35 U.S.C. §112, second paragraph is respectfully requested.

Claims 1, 3, 4, 8, 10, and 11 remain rejected as being obvious in view of previously-applied Gold. This rejection is respectfully traversed.

The problem addressed by Gold relates to the memory cell access delay associated with "wire length connecting a memory cell to the decode circuitry." Paragraph 0005. Gold notes that in this context, physical mapping and logical mapping of a memory cell are not always consistent. *Id.* Gold concludes that built-in self-test (BIST) technology is too complex and burdensome for "a memory array that lacks a consistent logical and physical address mapping." Paragraph 0006. Gold's invention then focuses on one particular memory array that contains cells with a logical mapping different from their physical mapping. Paragraph 0007. Gold's test generator generates a physical address for the memory array and a corresponding test factor. A conversion circuit 24 converts the physical address into a logical address, and the test vector is written to the logical address "to perform neighborhood pattern sensitive tests on physically adjacent cells." Paragraph 0010.

Thus, Gold's system relates to customized self-test of a single memory (i.e., embedded memory 28) in which the physical mapping and the logical mapping of the memory cells **within** that memory are not always consistent. Gold's address converter 24 compensates for any internal consistency in the mapping that particular memory.

In response to the Examiner's statements in paragraphs 5 and 6 of the Official Action, the independent claims have been amended to specifically recite that the system comprises a plurality of *different memories* having *different mappings* between physical memory locations and logical addresses associated with the physical memory locations. These amendments underscore the advantageous re-use of the claimed self-test controller for different memories having different physical-logical mappings. For example, claim 1 now recites "a plurality of different memories," with the "plurality of different memories having different mappings between physical memory locations and logical addresses associated with said physical memory locations." The self-test controller controls self-test of the plural different memories. Claim 1 also now recites "a plurality of mapping circuits, each of said plurality of mapping circuits corresponding to a respective one of said plurality of different memories." The plurality of different memories have "different mapping between physical memory locations and logical addresses associated with said physical memory locations." Applicant respectfully submits that the admitted distinctions between Gold and the present invention are now clearly recited in the independent claims. As the Examiner recognizes, Gold does not disclose the plurality of different memories or a mapping circuit provided for each of these different memories. The independent claims specify that the different memories have different mappings between physical memory locations and logical addresses associated with those physical memory locations. These features are neither disclosed nor suggested in Gold.

In paragraph 6 of the Official Action, the Examiner contends that it would have been obvious to "duplicate" Gold's address converter 24 and embedded memory 28 to arrive at a system with a plurality of memories, each having a mapping circuit. Applicant disagrees. Gold provides no motivation to use the BIST engine 20 with any other memory than the particular

embedded memory 28 with which it is associated. Furthermore, Gold teaches that the purpose of the address converter 24 is to compensate for inconsistencies in the physical mapping and the logical mapping of a memory cell within the single embedded memory 28 (see Gold page 1, paragraph 0005). There is no suggestion of re-using the BIST engine 20 for different memories. In Gold's system, there is no need to adapt values and timings for signals passed between the BIST engine and the embedded memory 28 because the BIST engine 20 is pre-configured with test and control functions specifically tailored to test the one particular embedded memory 28. There is no hint in Gold of an interface circuit that adapts values and timings of signals passed between a self-test controller and a plurality different memories to accommodate value and timing properties of the plurality of different memories.

It is not enough for the Examiner to simply point out that there could be a modification to Gold, i.e., the "duplication" proposed by the Examiner. Rather, the Federal Circuit has made it clear the prior art as a whole must suggest the desirability of such a modification. *In Re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998). Indeed, even a contention that a modification is a "trade off' is not a sufficient motivation. *Winner Int'l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 (Fed. Cir. 2000) ("Trade-offs often concern what is *feasible*, not what is, on balance, *desirable*." Motivation to combine requires the latter (emphasis added)).

The Examiner contends that Gold "implicitly" teaches adaptation of values and timings of signals passed between the BIST engine 20 and the embedded memory 28 because Gold teaches at paragraph 0017 that the address converter 24 may support built-in self-repair of the embedded memory array 28. The Examiner deduces from this statement that built-in self-repair circuits "inherently" adapt the repair circuits to the memory timing through synchronization of

signals interfacing to the memory array. But Gold neither discloses nor suggests how the address converter 24 would actually be adapted to support such built-in self-repair.

Indeed, memory defects must first be identified before any self-repair can be performed. Gold must actually perform the self-test operations to test the memory cells for defects in order to identify those defects and then repair them. Thus, the built-in self-repair disclosed by Gold relates to operations performed in a standard operational mode of the circuit *subsequent to* the self-test procedure. In contrast, the claimed adaptation of values and timings of signals is performed during the self-test process itself, and not in the standard operational mode of the system.

As a result of these differences, the claimed self-test controller is adaptable for use with a plurality of different memories based on generation of a single set of physical memory address signals. Providing a mapping circuit for each of the plurality of different memories allows the single set of physical memory address signals generated by the self-test controller to be readily adapted and translated to corresponding logical memory address signals appropriate for the particular memory with which the mapping circuit is associated. Thus, a single test generated by the self-test controller based on physical memory locations can be translated and applied to a plurality of different memories without requiring a complex self-test controller capable of generating different memory address signals appropriate for the set up and configuration of each of the plurality of different memories under test. Given its generic nature, the claimed self-test controller can adapt values and timings of signals passed between the self-test controller and the plurality of different memories to accommodate the particular properties of those different memories.

The application is in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____
John R. Lastova
Reg. No. 33,149

JRL:sd
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100